The aim of this thesis is to investigate possibilities for creating parallel arithmetic coding implementation and measure performance improvements.

In the first part, short overview of Arithmetic coding with its serial implementation (FastAC by Amir Said) is presented. The thesis then describes principles of work with GPUs and identifies possibilities of algorithm improvement and parallelization. Several parallel implementations are given, with varying performance improvements and occasional drawbacks.

In conclusion, thesis provides results of performance tests of our implementation, as well as discussion about feasibility of applying GPU-oriented version of algorithm instead of serial one in real-world applications.