

In this thesis we have added support for RISC-V into the MSIM emulator. MSIM supported only the MIPS R4000 as a CPU, and has been used for teaching the Operating systems course. This project redesigns MSIM to support multiple CPU architectures and adds an implementation of a RISC-V CPU. RISC-V as an architecture provides a basic instruction set as well as a wide variety of optional extensions. One chapter of this thesis is dedicated to giving an overview of the most important parts of the RISC-V architecture. The extensions that were thought to be useful or necessary for the Operating systems course have been implemented.