The thesis evaluates the viability of reducing power consumption of a contemporary computer cluster by using more power-efficient hardware components.

The cluster in question runs an Map-Reduce algorithm implementation and the worker nodes consist of either systems with an ARM CPU or systems which combine both an ARM CPU and an FPGA in a single package. The behavior of such cluster is discussed from both performance side as well as power consumption side.

The text discusses the problems and peculiarities with the integration of an ARM-based and especially the combined ARM-FPGA-based systems into the Map-Reduce framework. The Map-Reduce framework performance itself is evaluated to identify the gravest performance bottlenecks when using the framework in the environment with ARM systems.